Octal, 12-/16-Bit DAC, SPI, 5 ppm/°C On-Chip Reference in 4mm X 4mm LFCSP

Preliminary Technical Data

AD5628/AD5668 Package Note

FEATURES

Low power, pin-compatible octal DACs
- **AD5668: 16 bits**
- **AD5628: 12 bits**

AD5668/AD5628 in 16-lead LFCSP
On-chip 1.25 V/2.5 V, 5 ppm/°C reference
Power down to 400 nA @ 5 V, 200 nA @ 3 V
2.7 V to 5.5 V power supply
Guaranteed monotonic by design
Power-on reset to zero scale or midscale
3 power-down functions
Hardware $\overline{\text{LDAC}}$ and $\overline{\text{LDAC}}$ override function
$\overline{\text{CLR}}$ function to programmable code
Rail-to-rail operation

APPLICATIONS

Optical transceivers
Power Amp control
Data acquisition systems
Digital gain and offset adjustment

FUNCTIONAL BLOCK DIAGRAM

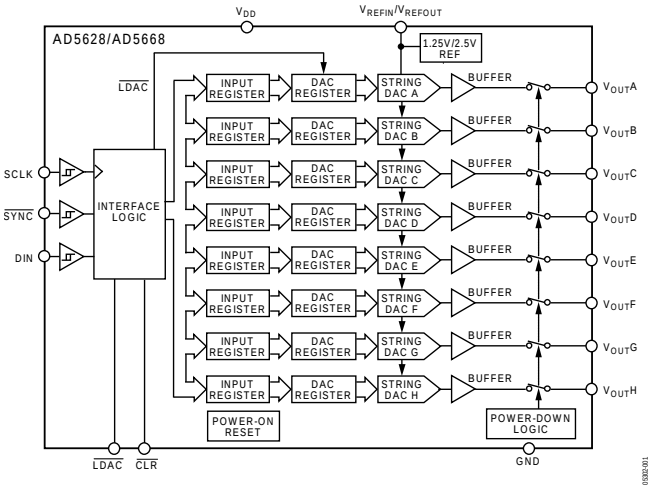

Figure 1.

GENERAL DESCRIPTION

The AD5628/AD5668 devices are low power, octal, 12-/16-bit, buffered voltage-output DACs. All devices operate from a single 2.7 V to 5.5 V supply and are guaranteed monotonic by design.

The AD5628/AD5668 have an on-chip reference with an internal gain of 2. The AD5628/AD5648/AD5668-1 have a 1.25 V 5 ppm/°C reference, giving a full-scale output range of 2.5 V; the AD5628/AD5668-2, -3 have a 2.5 V 5 ppm/°C reference, giving a full-scale output range of 5 V. The on-board reference is off at power-up, allowing the use of an external reference. The internal reference is enabled via a software write.

The part incorporates a power-on reset circuit that ensures that the DAC output powers up to 0 V (AD5628/AD5668-1, -2) or midscale (AD5668-3) and remains powered up at this level until a valid write takes place. The part contains a power-down feature that reduces the current consumption of the device to 400 nA at 5 V and provides software-selectable output loads while in power-down mode for any or all DAC channels.

The outputs of all DACs can be updated simultaneously using the $\overline{\text{LDAC}}$ function, with the added functionality of user-selectable DAC channels to simultaneously update. There is also an asynchronous $\overline{\text{CLR}}$ that updates all DACs to a user-programmable code—zero scale, midscale, or full scale.

The AD5628/AD5668 utilize a versatile 3-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with standard SPI®, QSPI™, MICROWIRE™, and DSP interface standards. The on-chip precision output amplifier enables rail-to-rail output swing.

PRODUCT HIGHLIGHTS

1. Octal, 12-/16-bit DAC.
2. On-chip 1.25 V/2.5 V, 5 ppm/°C reference.
3. Available in 16-lead LFCSP.
4. Power-on reset to 0 V or midscale.
5. Power-down capability. When powered down, the DAC typically consumes 200 nA at 3 V and 400 nA at 5 V.

Rev PrA
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PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

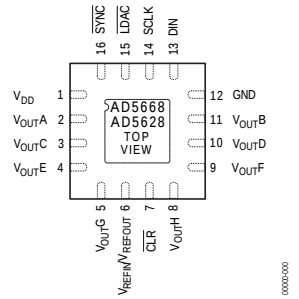
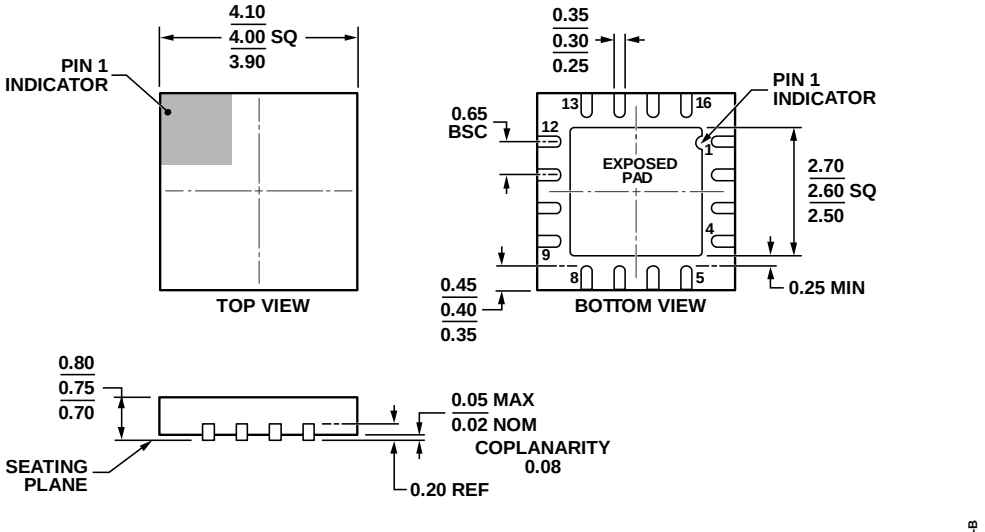


Figure 2. 16-Lead LFCSP (CP-16-17)

Table 1. Pin Function Descriptions

16-Lead LFCSP	Mnemonic	Description
15	$\overline{\text{LDAC}}$	Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows all DAC outputs to simultaneously update. Alternatively, this pin can be tied permanently low.
16	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and enables the input shift register. Data is transferred in on the falling edges of the next 32 clocks. If $\overline{\text{SYNC}}$ is taken high before the 32nd falling edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the device.
1	V_{DD}	Power Supply Input. These parts can be operated from 2.7 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
2	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
11	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
3	$V_{OUT}C$	Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
10	$V_{OUT}D$	Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
6	V_{REFIN}/V_{REFOUT}	The AD5628/AD5648/AD5668 have a common pin for reference input and reference output. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference input.
7	$\overline{\text{CLR}}$	Asynchronous Clear Input. The $\overline{\text{CLR}}$ input is falling edge sensitive. When $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is activated, the input register and the DAC register are updated with the data contained in the $\overline{\text{CLR}}$ code register—zero, midscale, or full scale. Default setting clears the output to 0 V.
4	$V_{OUT}E$	Analog Output Voltage from DAC E. The output amplifier has rail-to-rail operation.
9	$V_{OUT}F$	Analog Output Voltage from DAC F. The output amplifier has rail-to-rail operation.
5	$V_{OUT}G$	Analog Output Voltage from DAC G. The output amplifier has rail-to-rail operation.
8	$V_{OUT}H$	Analog Output Voltage from DAC H. The output amplifier has rail-to-rail operation.
12	GND	Ground Reference Point for All Circuitry on the Part.
13	DIN	Serial Data Input. This device has a 32-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
14	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.

OUTLINE DIMENSION



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 2. 16-Lead Frame Chip Scale Package [LFCSP]
(CP-16-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Power-On Reset to Code	Accuracy	Internal Reference
AD5628ACPZ-1	−40°C to +105°C	16-Lead LFCSP	CP-16-17	Zero	±2 LSB INL	1.25V
AD5628ACPZ-2	−40°C to +105°C	16-Lead LFCSP	CP-16-17	Zero	±2 LSB INL	2.5V
AD5628BCPZ-2	−40°C to +105°C	16-Lead LFCSP	CP-16-17	Zero	±1 LSB INL	2.5V
AD5668ACPZ-2	−40°C to +105°C	16-Lead LFCSP	CP-16-17	Zero	±32 LSB INL	2.5V
AD5668ACPZ-3	−40°C to +105°C	16-Lead LFCSP	CP-16-17	Midscale	±32 LSB INL	2.5V
AD5668BCPZ-1	−40°C to +105°C	16-Lead LFCSP	CP-16-17	Zero	±16 LSB INL	1.25V
AD5668BCPZ-2	−40°C to +105°C	16-Lead LFCSP	CP-16-17	Zero	±16 LSB INL	2.5V
EVAL-AD5668EBZ-CP		LFCSP Evaluation board				

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